EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Phillip J. Articola (Registration#38,819) on 06/11/2010.

The application claims have been amended as follows:

1. (currently amended) A data processing apparatus that has a plurality of reception interface sections which receive same data from a same data sender and processes data, received by said plurality of reception interface sections, in parallel, comprising:

a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of said reception interface sections and said data sender,

wherein each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal,

wherein each of said reception interface sections includes a communication error processing section which, upon occurrence of an error in said received data by one of said reception interface sections, stops receiving said data, sends a communication

error signal to all other of said reception interface sections to stop data reception from said data sender, and requests said data sender to resend data,

wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of the respective reception interface section,

wherein said error in said received data is detected by said memory bridge of said one of said reception interface sections, and

wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections~~.~~ , and further comprising:

a transaction layer that receives the communication error signal output from the communication error processing section;

an internal circuit section; and

a synchronization buffer that exchanges data between the transaction layer and the internal circuit section,

wherein the internal circuit section acquires data held in the synchronization buffer at a timing synchronous with said sync signal and sends the acquired data to a processor external to the data processing apparatus.

Claim 6. (canceled)

7. (currently amended) A data processing method of a data processing apparatus that performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender and comprises:

a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender;

a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal;

an error detection step of detecting an error in said received data by one of said reception interface sections; and

an error information output step of outputting information on said detected error by said one of said reception interface sections to all other of said reception interface sections,

wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of said respective reception interface section,

wherein said error detection step comprises detecting said error in said received data by said memory bridge of said one of said reception interface sections, and

wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected

error to said other memory bridges of said other reception interface sections~~.~~ , and further comprising: receiving, by a transaction layer, a communication error signal output in the error information output step;

exchanging data, by a synchronization buffer, between a transaction laver and an internal circuit section, wherein the internal circuit section acquires data held in the synchronization buffer at a timing synchronous with said sync signal; and

sending the acquired data by the internal circuit section to a processor external to the data processing apparatus.

12. (currently amended) A non-transitory computer readable medium having thereon a computer program, which when executed, performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender and allows a ~~computer~~ data processing apparatus to execute:

a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender;

a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal;

an error detection step of detecting an error in said received data by one of said reception interface sections; and

an error information output step of outputting information on said detected error by said one of said reception interface sections to all other of said reception interface sections,

wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of said respective reception interface section,

wherein said error detection step comprises detecting said error in said received data by said memory bridge of said one of said reception interface sections, and

wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections~~.~~, and wherein said data processing apparatus is allowed to further execute: receiving, by a transaction layer, a communication error signal output in the error information output step;

exchanging data, by a synchronization buffer, between a transaction laver and an internal circuit section, wherein the internal circuit section acquires data held in the synchronization buffer at a timing synchronous with said sync signal; and

sending the acquired data by the internal circuit section to a processor external to the data processing apparatus.

14. (currently amended) The computer readable medium according to claim 13, wherein said ~~computer~~ data processing apparatus is allowed to further execute:

an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections; and a data resend requesting step of requesting said data sender to resend data in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step.

15. (currently amended) The computer readable medium according to claim 14, wherein said ~~computer~~ data processing apparatus is allowed to further execute:

a data cancellation step of canceling data; and

a data reception stopping step of stopping data reception, and

said data cancellation step and said data reception stopping step are executed in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step, and

said data resend requesting step requests resending of data canceled at said data cancellation step.

Claims 20 and 21. (canceled)

End of Amendment.

Reasons For Allowance

2. Claims 1-4 and 7-19 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Regarding independent claim **1**, prior art of record fails to teach or render obvious, alone or in combination, a data processing apparatus that has a plurality of reception interface sections which receive same data from a same data sender and processes data, received by said plurality of reception interface sections, in parallel, comprising: a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of said reception interface sections and said data sender, wherein each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal, and wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections and further comprising: *receiving, by a transaction layer, a communication error signal output in the error information output step; exchanging data, by a synchronization buffer, between a transaction laver and an internal circuit section, wherein the internal circuit section acquires data held in the synchronization buffer at a timing synchronous with said sync signal; and sending the acquired data by the internal circuit section to a processor external to the data processing apparatus*, in combination with all other disclosed limitations as recited in independent claim 1.

Regarding independent claim **7**, prior art of record fails to teach or render obvious, alone or in combination, a data processing method of a data processing apparatus that performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender and comprises: a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender; a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal; and wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections, and *further comprising: receiving, by a transaction layer, a communication error signal output in the error information output step; exchanging data, by a synchronization buffer, between a transaction laver and an internal circuit section, wherein the internal circuit section acquires data held in the synchronization buffer at a timing synchronous with said sync signal; and sending the acquired data by the internal circuit section to a processor external to the data processing apparatus*, in combination with all other disclosed limitations as recited in independent claim 7.

Regarding independent claim **12**, prior art of record fails to teach or render obvious, alone or in combination, a non-transitory computer readable medium having thereon a computer program, which when executed, performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender and allows a data processing apparatus to execute: a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender; a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal; and wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections, and wherein said data processing apparatus is allowed to further execute: *receiving, by a transaction layer, a communication error signal output in the error information output step; exchanging data, by a synchronization buffer, between a transaction laver and an internal circuit section, wherein the internal circuit section acquires data held in the synchronization buffer at a timing synchronous with said sync signal; and sending the acquired data by the internal circuit section to a processor external to the data processing apparatus*, in combination with all other disclosed limitations as recited in independent claim 12.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any response to this office action should be faxed to (571) 273-8300 or mailed To:

Commissioner for Patents,

P.O. Box 1450

Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22314.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SRINIVASA R. REDDIVALAM whose telephone number

is (571)270-3524. The examiner can normally be reached on Mon-Fri 9:30 AM - 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on 571-272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srini Reddivalam

06/11/2010

/Chirag G Shah/

Supervisory Patent Examiner, Art Unit 2477